AMENDMENTS TO THE SPECIFICATION

The following is a marked up version of each replacement paragraph and/or section of the specification in which underlines indicate insertions and strikethrough indicates deletions.

On page 5, please replace the paragraph containing lines 22-31, with the following paragraphs:

Each of the sixteen data registers is connected to a respective one of sixteen pipelines. FIG. 3 shows only the pipelines 40, 41, 42, and 43, which are connected to respective data registers 30, 31, 32, and 33. After two data registers 30 and 32 received data in response to column cycle signal COLCYC<0>, the two data [[resistors]] registers 30 and 32 transmit the data bits to pipelines 40 and 42. The pipelines 40 and 42 sequentially transmit data bits from each stage to the succeeding stage in a transmission operation in response to a clock signal (not shown). The pipelines 40 and 42 serially transmit the output data DATA to channel bus lines C_DQA0 and C_DQB0 through the output driers 50 and 52, respectively. Accordingly, one RDRAM 11 outputs two data bits, one bit applied to each of the channel bus lines C_DQA0 and C_DQB0.